

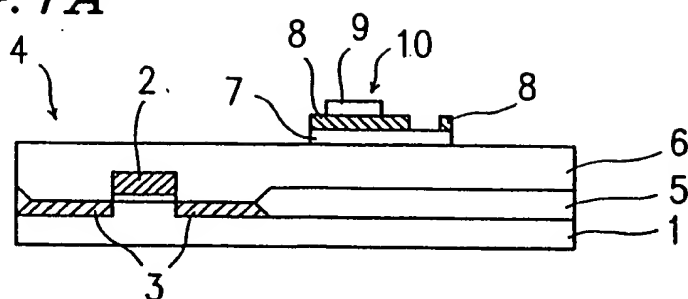
[illegible]

FIG. 1B

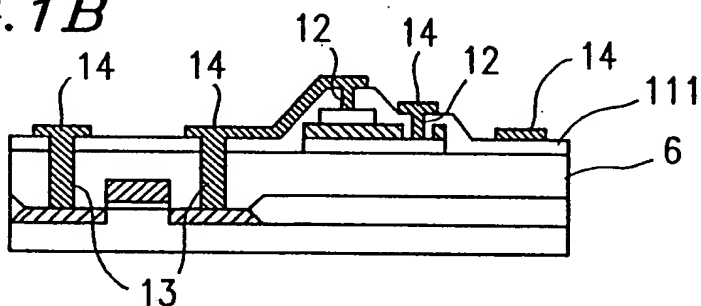


FIG. 1C

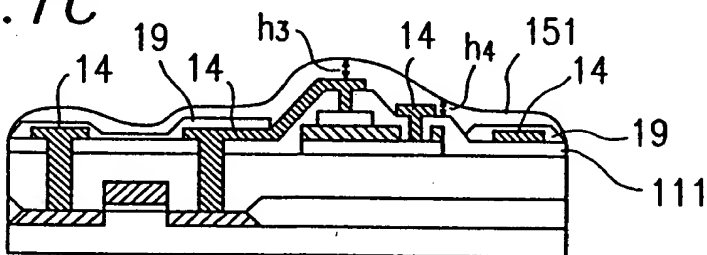


FIG. 1D

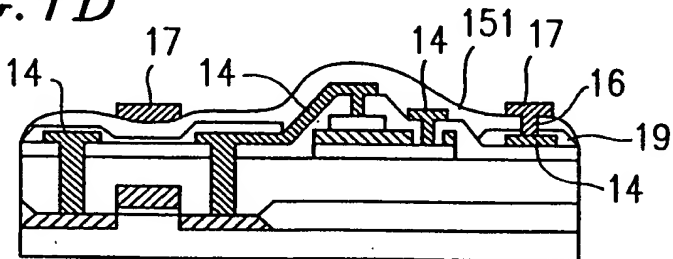


FIG. 1E

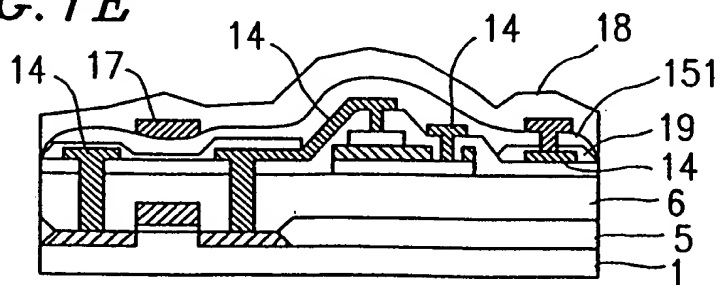
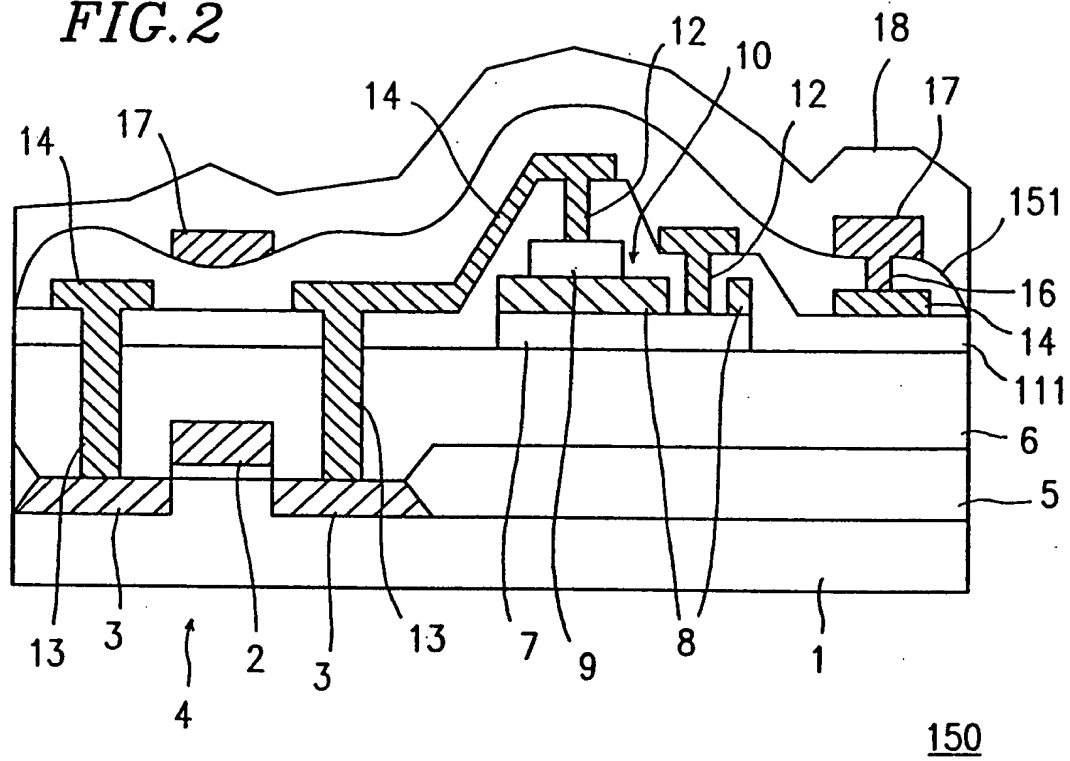
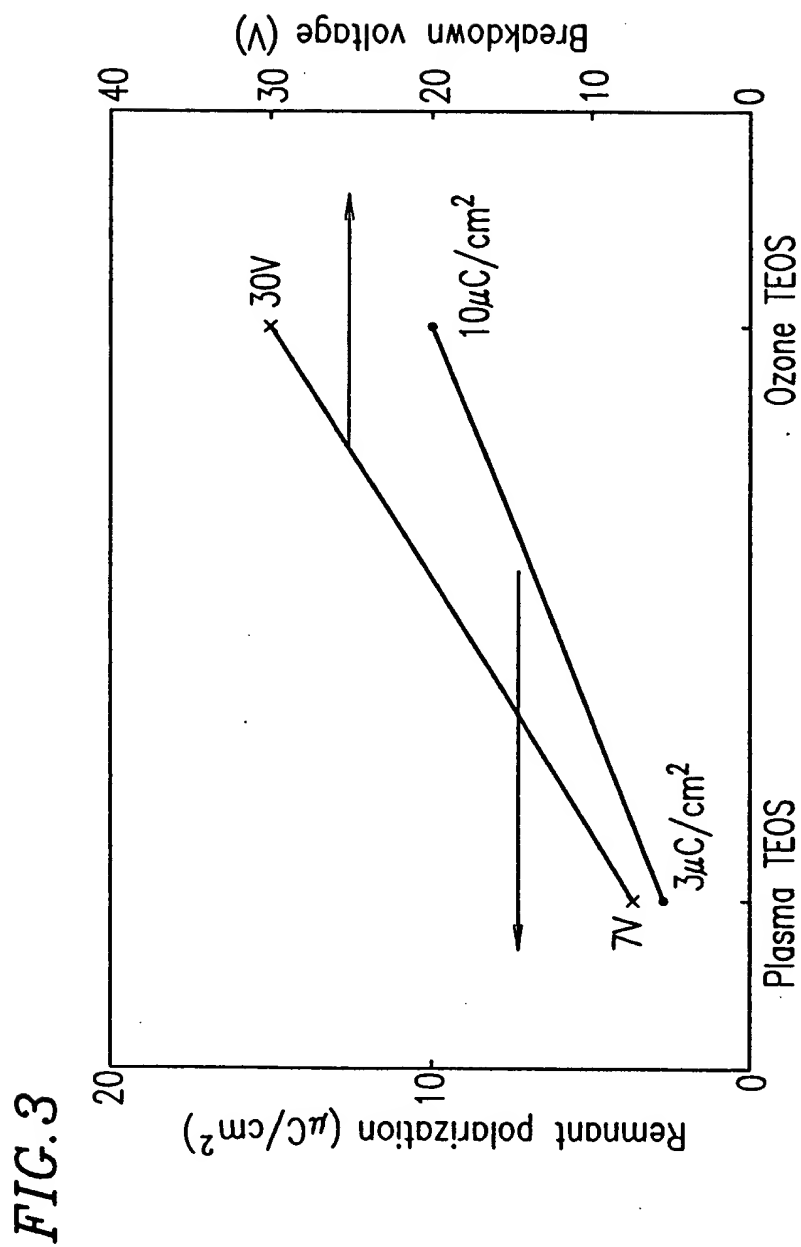


FIG. 2





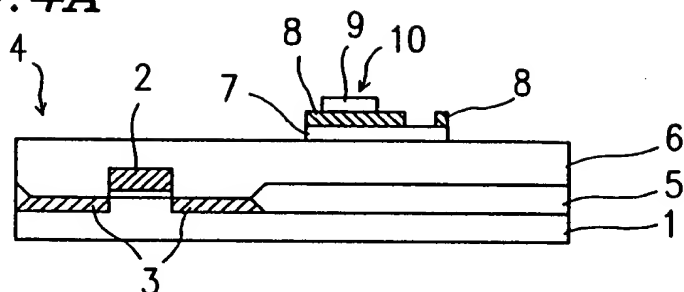
[illegible]

FIG. 4B

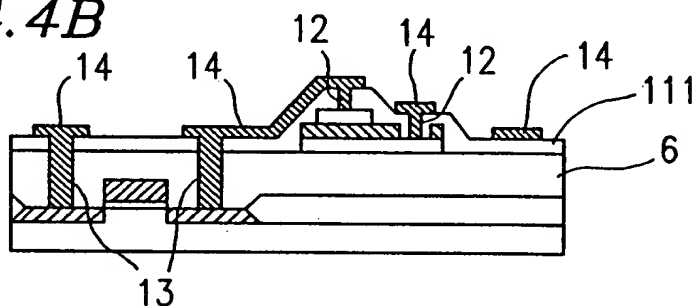


FIG. 4C

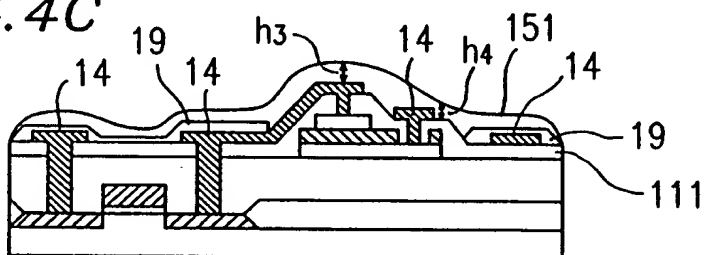


FIG. 4D

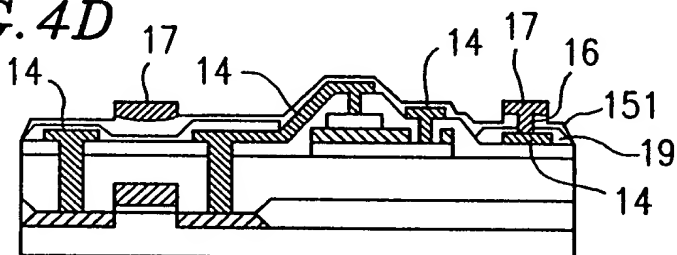
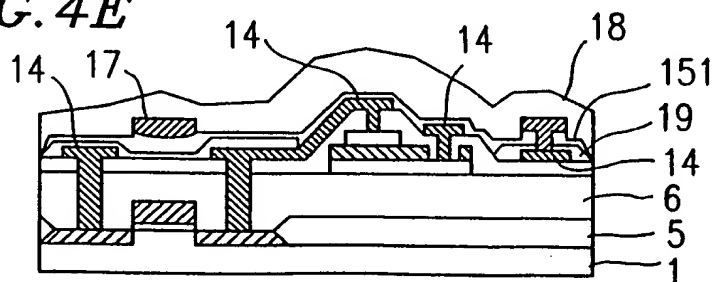


FIG. 4E



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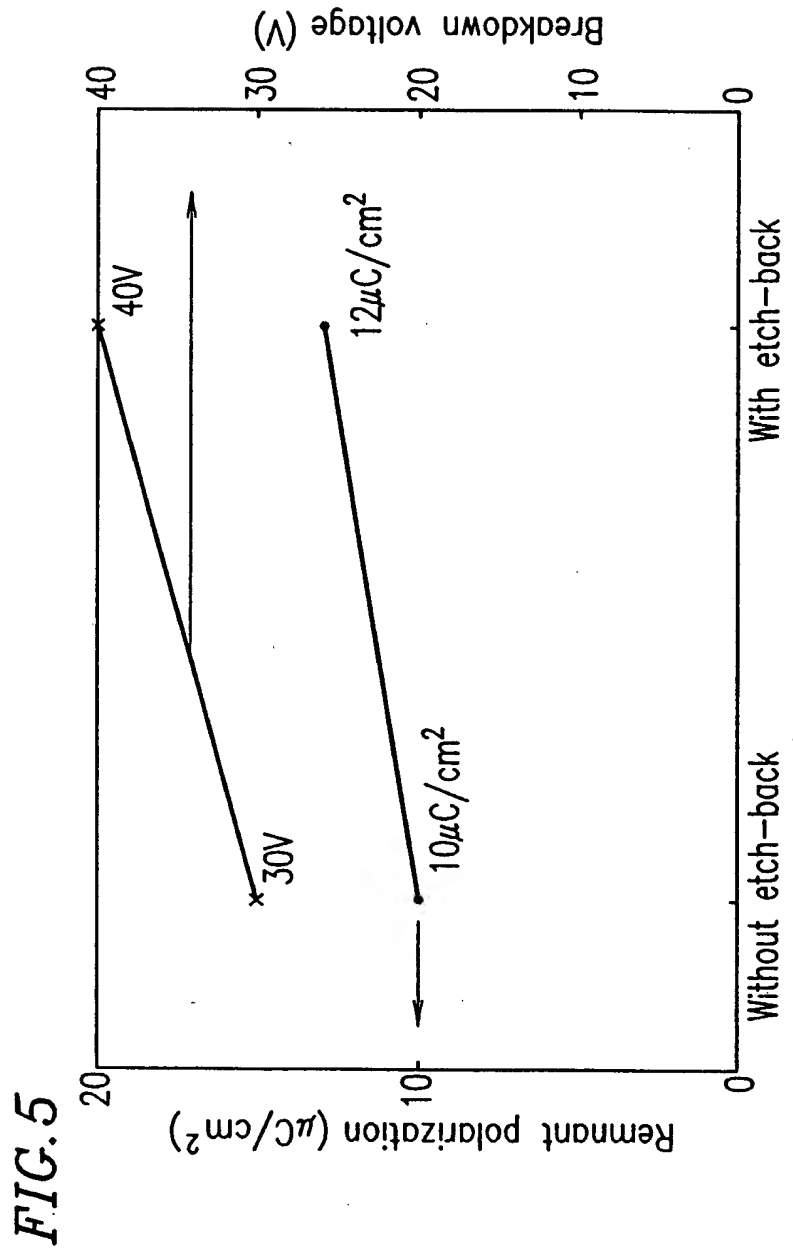


FIG. 6A

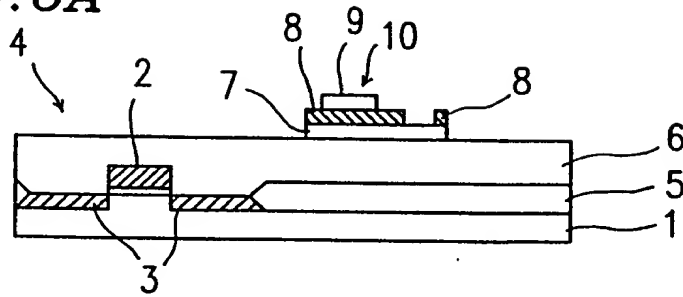


FIG. 6B

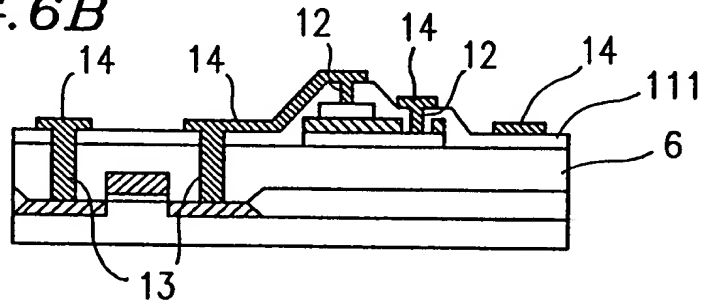


FIG. 6C

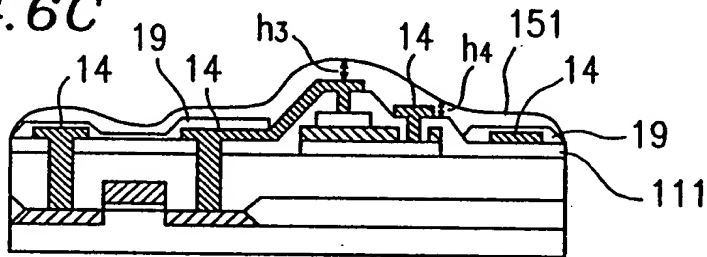


FIG. 6D

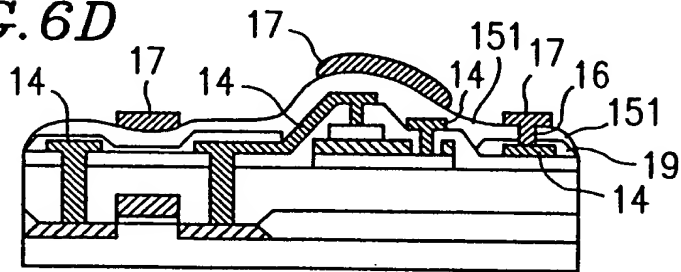
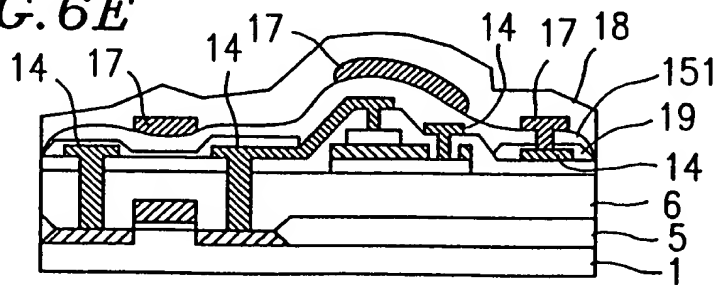


FIG. 6E



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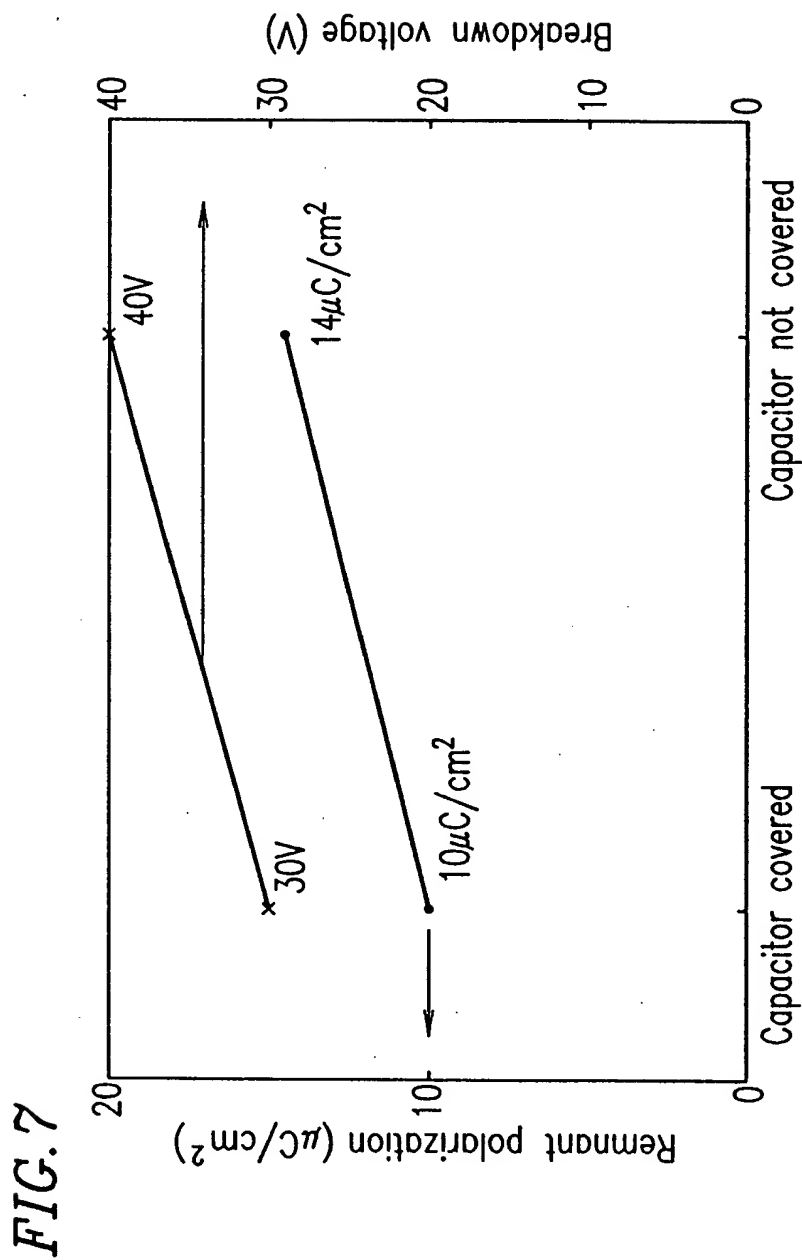
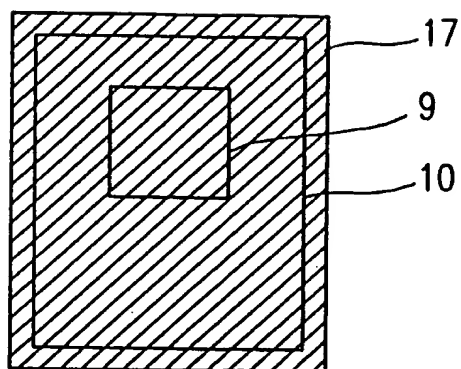
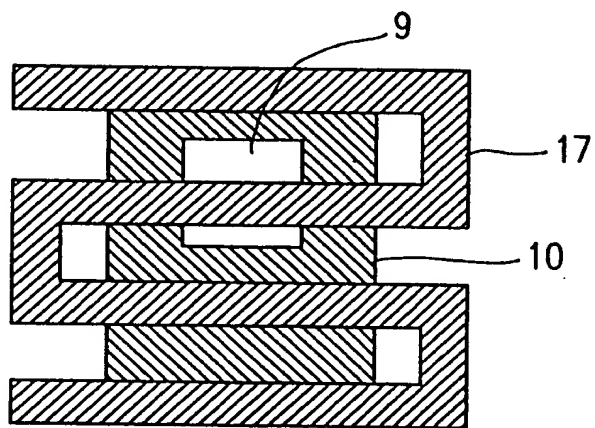
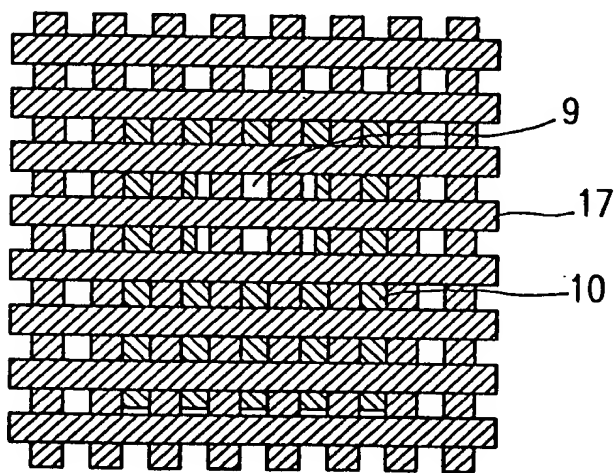


FIG. 8A*FIG. 8B**FIG. 8C*

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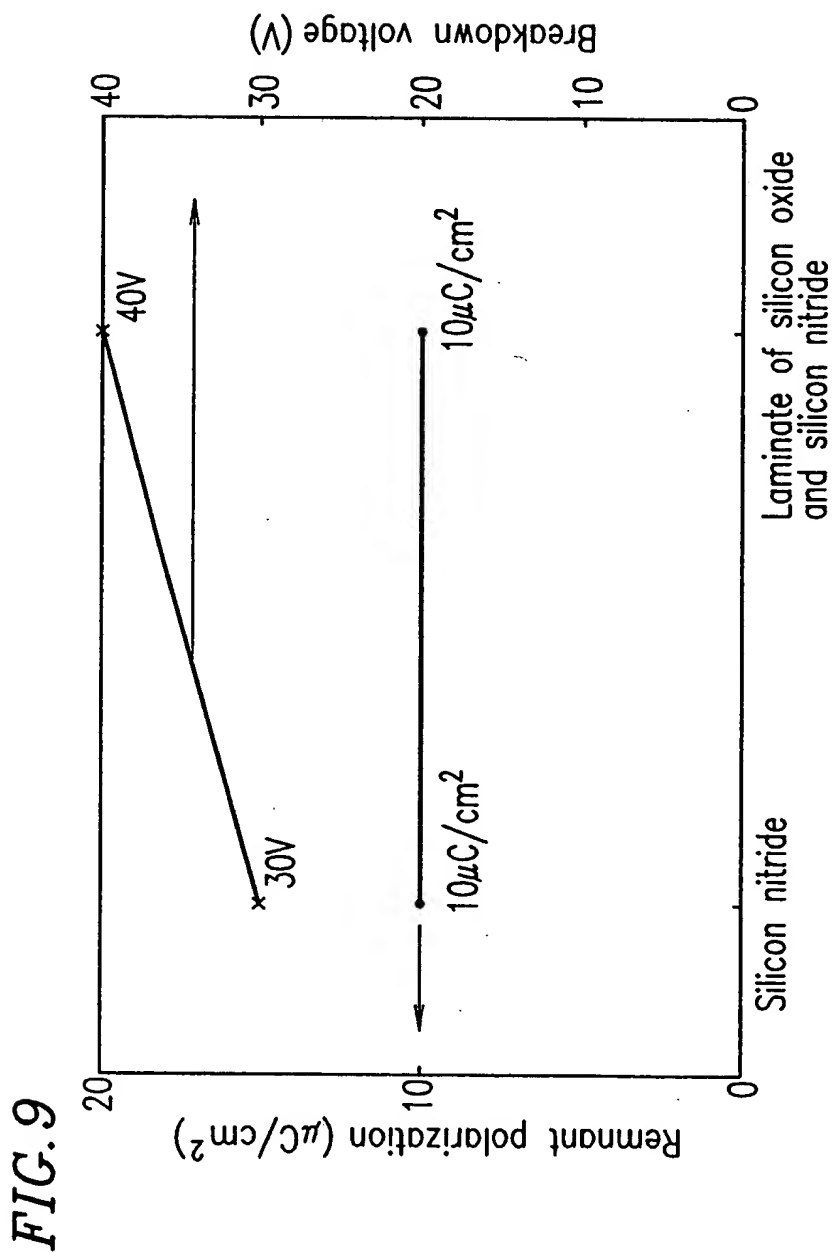


FIG. 70A is a cross-sectional view of a semiconductor device. The device consists of a substrate with three distinct layers labeled 1, 5, and 6. A central region of the substrate contains a stack of three layers: a bottom layer labeled 3, a middle layer labeled 2, and a top layer labeled 4. To the right of this central stack, there is another structure consisting of a bottom layer labeled 7, a middle layer labeled 8, and a top layer labeled 9. A small feature, also labeled 8, is located on the right side of the substrate, adjacent to the structure with layers 7, 8, and 9. A layer labeled 10 is shown as a thin layer on top of the structure with layers 7, 8, and 9.

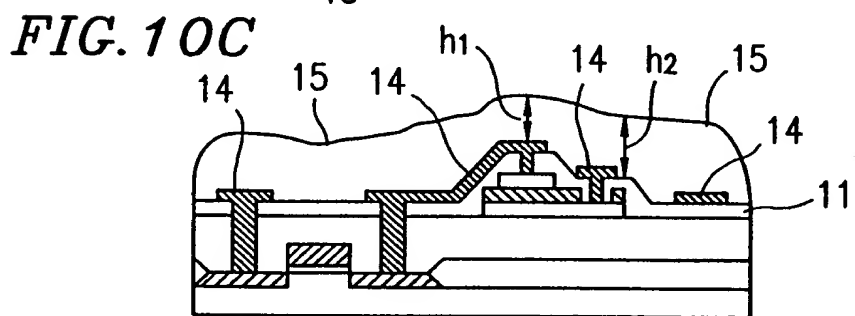


FIG. 70D is a cross-sectional view of a semiconductor device. It shows a substrate with multiple layers labeled 14, 15, and 16. A central structure 18 is formed on the substrate, consisting of several stacked layers and a top layer 17. The structure 18 is surrounded by a material 15, which is further covered by a layer 16. The top surface of the device is covered by a layer 17, which has a central opening or gap. The device is shown in a cross-sectional view, with the layers and structures labeled with reference numerals.

FIG. 10E

FIG. 10E is a cross-sectional view of a semiconductor device. It shows a substrate with layers 1, 5, and 6. A central structure includes a gate stack (11) and a channel region (17) with a p+ region (18) on top. A source/drain region (17) is also shown on the right side.

[illegible]

FIG. 11A

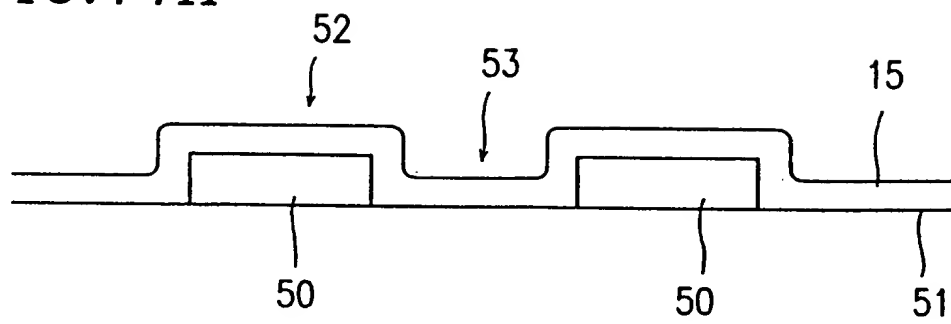


FIG. 11B

